AMENDMENTS TO THE SPECIFICATION

Please replace paragraph **[0011]** in the specification with the following amended paragraph.

[0011] These and other objects of the present invention may be achieved by an efficient implementation of a decision directed phase locked loop (DD-PLL), comprising: an enhanced block decoder inside a phase detector which takes in the baseband complex samples and the current channel phase estimate (or the tracked phase) and generates a feedback phase error term; a loop filter which filters the phase error terms; and a phase accumulator that updates the tracked phase estimate on each iteration of [[he]]the loop.

Please insert the following paragraph immediately proceeding paragraph **[0020]** in the specification.

Fig. 8 illustrates a communication receiver including an implementation of an improved phase detector according to the invention.

Please replace paragraph **[0029]** in the specification with the following amended paragraph.

[0029] In order to improve the performance of the decision directed phase locked loop (DD-PLL) at low signal-to-noise ratios, an improved decision directed phase locked loop (DD-PLL) has been proposed in U.S. Patent No. 6,236,687, commonly assigned to ~~TRW Inc~~Northrop Grumman Corp., the assigned of this patent application, and hereby incorporated by reference in its entirety, that utilizes a block decoder inside the phase locked loop. More specifically, it is the phase detector component of the phase locked loop that is improved (see element 22-2' in FIG. 3). As is known from the subject matter incorporated by reference, the improved decision directed phase locked loop (DD-PLL) comprises a block decoder, such as a Reed-Muller block decoder, for decoding the set of vector pairs of phase stabilized observables in rectangular form at a decode rate to generate decoded data. The decoded data at each codeword is provided to the loop filter 22-3 to yield an update of an estimated phase at every codeword.

Please insert the following paragraphs immediately proceeding paragraph **[0051]** in the specification.

Fig. 8 illustrates an example of a communication receiver 50 using a demodulator for receiving an input modulated signal, which could be a BPSK or a QPSK modulated signal, from a transmission channel which is encoded by a sequence of codewords corresponding to biorthogonal binary codes. Each of the codewords could contain four data symbols. The communication receiver 50 comprises a down converter 52 which is operative to down convert the input modulated signal into an intermediate frequency signal that is a baseband quadrature pair including an in-phase (I) component and a quadrature-phase (Q) component. A synchronous demodulator 54 demodulates the intermediate frequency signal from a baseband quadrature pair into a sequence of complex sample pairs. A matched filter and sampler 56 passes the sequence of complex sample pairs and produces a succession of baseband signal samples by passing the sequence of complex sample pairs and sampling them at a symbol rate.

The communication receiver 50 also includes a rectangular to polar converter 58 which converts the succession of baseband signal samples of the input modulated signal from a rectangular form into a pair of polar coordinates having an incoming phase, and a phase locked loop 60 which estimates the phase of the input modulated signal. The phase locked loop 60 comprises a comparator 62 which generates a phase difference of the incoming phase of the input modulated signal and an estimated phase. The phase locked loop 60 includes a polar to rectangular converter 64 which converts the polar coordinates having the phase difference into a set of vector pairs of phase stabilized observables in the rectangular form. The comparator 62 in the communication receiver 50 could be a subtractor for substracting the incoming phase of the input modulated signal from the estimated phase to generate the phase difference. The phase locked loop 60 also includes a block decoder 66 which decodes the set of vector pairs of phase stabilized observables in the rectangular form at a decode rate that could be one quarter of the symbol rate to generate decoded data and a phase error estimate. The phase locked loop 60 also may include a loop filter 68 which filters the phase error estimate from the block decoder 66 to yield an update of the estimated phase at each codeword.

The communication receiver 50 of Fig. 8 should not be limited to that which is described above. For example, the block decoder 66 depicted in Fig. 8 could be a Reed-Muller decoder that determines the phase error estimate based on the composite decoded codeword phase error relative to a reference value. The estimated phase could be updated at a rate that is one quarter the symbol rate or every codeword of four data symbols.